

- Hot Plug Protection
- Quad 0.5 to 1.3 Gigabits Per Second (Gbps) Serializer/Deserializer
- Independent Channel Operation
- 2.5-V Power Supply for Low Power Operation
- Selectable Signal Preemphasis for Serial Output
- Interfaces to Backplane, Copper Cables, or Optical Converters
- Lock Indication and Sync Mode for Fast Initialization
- 18-Bit Parallel Buses for Flexible Interface Applications
- On-chip PLL Provides Clock Synthesis From Low-Speed Reference
- Receiver Differential Input Thresholds 200 mV Min
- Rated for Industrial Temperature Range
- Typical Power: 1150 mW at 1.3 Gbps
- Ideal for High-Speed Backplane Interconnect and Point-to-Point Data Link
- Internal Passive Receive Equalization
- Small Footprint 19 mm x 19 mm, 289-Ball PBGA Package

description

The TLK4120 is a four channel, multi-gigabit transceiver used in high-speed bidirectional point-to-point data transmission systems. The TLK4120 supports an effective serial interface speed of 0.5 Gbps to 1.3 Gbps per channel, providing up to 1.17 Gbps of data bandwidth per channel.

The primary application of the TLK4120 is to provide high-speed I/O data channels for point-to-point baseband data transmission over controlled impedance media of approximately 50 Ω . The transmission media can be a printed-circuit board, copper cables, or fiber-optic cable. The maximum rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The TLK4120 can also be used to replace parallel data transmission architectures by providing a reduction in the number of traces, connector pins, and transmit/receive pins. Parallel data loaded into the transmitter is delivered to the receiver over a serial channel, which can be a coaxial copper cable, a controlled impedance backplane, or an optical link. The data is then reconstructed into its original parallel format. It offers significant power and cost savings over current solutions, as well as scalability for higher data rate in the future.

The TLK4120 performs the data parallel-to-serial, serial-to-parallel conversion, and clock extraction functions for a physical layer interface device. The serial transceiver interface operates at a maximum speed of 1.3 Gbps. The transmitter latches 18-bit parallel data at a rate based on the supplied reference clock (GTx_CLK). The 18-bit parallel data is internally encoded into 20 bits by framing the 18-bit data with a start and a stop bit. The resulting 20-bit frame is then transmitted differentially at 20 times the reference clock (GTx_CLK) rate. The receiver section performs the serial-to-parallel conversion on the input data, synchronizing the resulting 20-bit wide parallel data to the recovered clock (Rx_CLK). It then extracts the 18 bits of data from the 20-bit wide data resulting in 18 bits of parallel data at the receive data terminals (RDx[0:17]). This results in an effective data payload of 0.45 Gbps to 1.17 Gbps (18 bits data x GTx_CLK frequency).

The TLK4120 is designed to be hot plug capable. An on-chip power-on reset circuit holds the Rx_CLK low and places the parallel side output signal terminals, DOUTrxP and DOUTrxN, into a high-impedance state during power up.

The TLK4120 uses a 2.5-V supply. The I/O section is 3-V compatible. With the 2.5-V supply, the TLK4120 is power efficient, consuming less than 1150 mW typically. The TLK4120 is characterized for operation from -40°C to 85°C .



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AVAILABLE OPTIONS

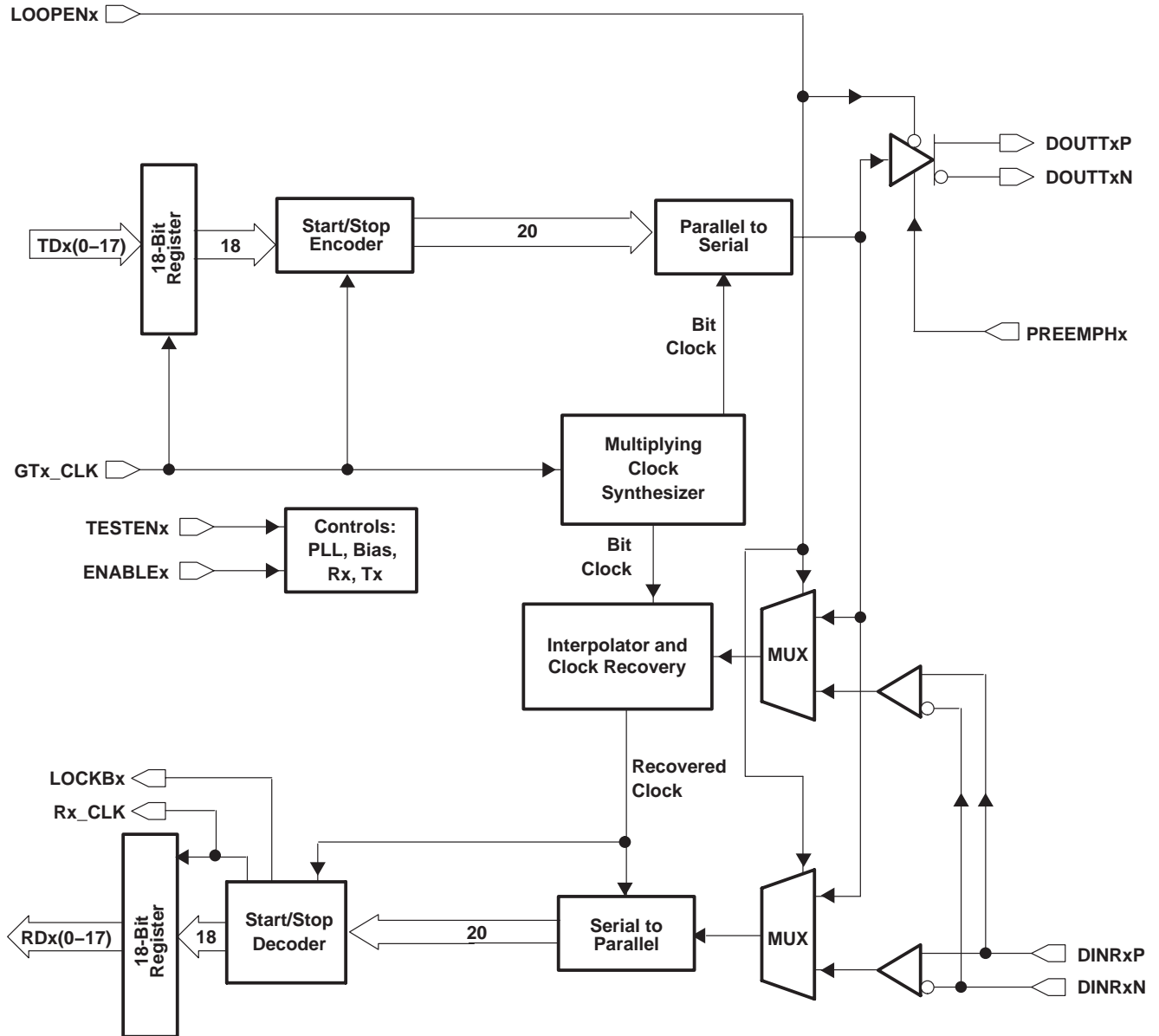
| | | |
|----------------------|---------------------------------------|---------------|
| T_A | PACKAGE | SYMBOL |
| | PLASTIC BALL GRID ARRAY (PBGA) | |
| -40°C to 85°C | TLK4120IGPV | |
| | TLK4120IZPV | ECAT |

NOTE: For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T | U | |
|----|----------------------|---------|----------------------|----------------------|----------------------|---------------------|--------------------|---------------------|---------------------|---------|----------------------|----------------------|----------------------|---------------------|--------|-------|----------------------|----|
| 17 | TDB1 | TDB0 | DOU _{TTB} P | DOU _{TTB} N | PREEMP _{HB} | DINRBP | DINRBN | RDB0 | GND | TDC0 | DOU _{TTC} P | DOU _{TTC} N | PREEMP _{HC} | DINRCP | DINRCN | RDC0 | RDC1 | 17 |
| 16 | TDB4 | TDB2 | GND | GND | VDDAB | GND | GND | RDB1 | VDD | TDC1 | GND | GND | VDDAC | GND | GND | RDC2 | RDC4 | 16 |
| 15 | TDB5 | TDB3 | GND | RDB3 | VDDAB | RDB2 | GND | VDD | GND | VDD | GND | TDC2 | VDDAC | VDD | GND | RDC3 | RDC5 | 15 |
| 14 | TDB7 | TDB6 | VDD | RB_CLK | RDB7 | RDB4 | RDB5 | RDB6 | GND | TDC5 | TDC6 | TDC7 | TDC4 | TDC3 | GND | RDC6 | RDC7 | 14 |
| 13 | TDB8 | GTB_CLK | GND | RDB17 | RDB13 | RDB10 | RDB9 | RDB8 | VDD | GTC_CLK | TDC9 | TDC10 | TDC11 | TDC14 | VDD | RDC8 | RC_CLK | 13 |
| 12 | TDB9 | TDB10 | VDD | SYNCB | RDB16 | RDB14 | RDB12 | RDB11 | VDD | TDC8 | TDC12 | TDC13 | TDC16 | LOOPEN _C | GND | RDC10 | RDC9 | 12 |
| 11 | TDB11 | TDB13 | GND | VDD | LOCKBB | RDB15 | GND | GND | GND | GND | GND | TDC15 | VDD | TESTEN _C | GND | RDC13 | RDC11 | 11 |
| 10 | TDB12 | GND | TDB15 | LOOPEN _B | ENABLE _B | TESTEN _B | GND | GND | GND | GND | GND | TDC17 | SYNCC | RDC17 | RDC14 | GND | RDC12 | 10 |
| 9 | TDB14 | TDB16 | GND | TDB17 | GND | VDD | GND | GND | GND | GND | GND | ENABLE _C | LOCKBC | GND | RDC16 | RDC15 | VDD | 9 |
| 8 | RDA0 | RDA1 | VDD | RDA6 | RDA8 | RDA11 | GND | GND | GND | GND | GND | TDD8 | VDD | GTD_CLK | TDD5 | TDD1 | TDD0 | 8 |
| 7 | DINRAN | GND | GND | RDA5 | RDA9 | RDA12 | GND | GND | GND | GND | GND | TDD12 | TDD9 | TDD6 | GND | GND | DOU _{TTD} P | 7 |
| 6 | DINRAP | GND | RDA2 | RDA4 | RDA10 | RDA14 | RDA15 | TESTEN _A | ENABLE _D | TDD17 | TDD15 | TDD13 | TDD10 | TDD7 | TDD2 | GND | DOU _{TTD} N | 6 |
| 5 | PREEMP _{HA} | VDDAA | VDDAA | RDA7 | RDA13 | RDA16 | LOCKB _A | ENABLE _A | GND | SYNCD | VDD | TDD16 | TDD11 | TDD4 | VDDAD | VDDAD | PREEMP _{HD} | 5 |
| 4 | DOU _{TTA} N | GND | RDA3 | RA_CLK | RDA17 | SYNCA | VDD | LOOPEN _A | TDA17 | RDD17 | LOCKBD | LOOPEN _D | TDD14 | TDD3 | VDD | GND | DINRDP | 4 |
| 3 | DOU _{TTA} P | GND | GND | VDD | GND | VDD | GND | TDA15 | RDD16 | RDD15 | GND | TESTEN _D | VDD | GND | GND | GND | DINRDN | 3 |
| 2 | TDA0 | TDA2 | TDA3 | TDA6 | GTA_CLK | TDA10 | TDA13 | GND | TDA16 | RDD14 | RDD13 | RDD10 | RDD8 | RDD6 | RDD3 | RDD2 | RDD0 | 2 |
| 1 | TDA1 | TDA4 | TDA5 | TDA7 | TDA8 | TDA9 | TDA11 | TDA12 | TDA14 | RDD12 | RDD11 | RDD9 | RD_CLK | RDD7 | RDD5 | RDD4 | RDD1 | 1 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T | U | |

functional block diagram

A detailed block diagram of each channel is shown below. Channels A, B, C, and D are identical and are configured as four separate links.



transmit interface

The transmitter portion registers valid incoming 18-bit wide data (TDx[0:17]) on the rising edge of GTx_CLK. The data is then framed with start and stop bits, serialized, and transmitted sequentially over the differential high-speed I/O channel. The clock multiplier multiplies the reference clock (GTx_CLK) by a factor of 10 creating a bit clock. This internal bit clock is fed to the parallel-to-serial shift register, which transmits data on both the rising and falling edges of the bit clock providing a serial data rate that is 20 times the reference clock. Data is transmitted LSB (TDx0) first.

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transmit data bus

The transmit bus interface accepts 18-bit wide single-ended TTL parallel data at the TDx[0:17] terminals. Data is valid on the rising edge of GTx_CLK. The GTx_CLK is used as the word clock. The data and clock signals must be properly aligned as shown in Figure 1. Detailed timing information can be found in the *TTL input electrical characteristics* table.

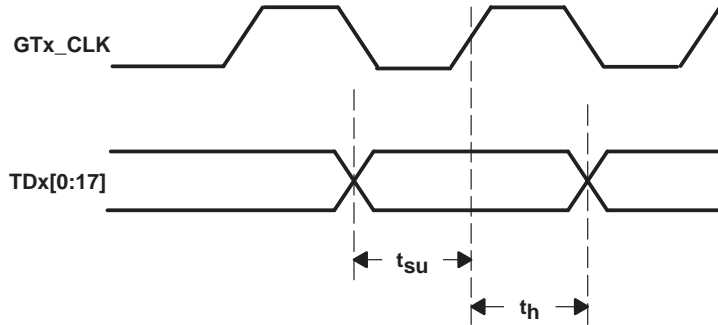


Figure 1. Transmit Timing Waveform

transmission latency

The data transmission latency of the TLK4120 is defined as the delay from the initial 18-bit word on the parallel transmit interface to the serial transmission of the start bit of the 20-bit frame containing the 18-bit word. The transmit latency is fixed once the link is established. However, due to silicon process variations and implementation variables, such as supply voltage and temperature, the exact delay varies slightly. Figure 2 illustrates the timing relationship between the transmit data bus, GTx_CLK, and serial transmit terminals.

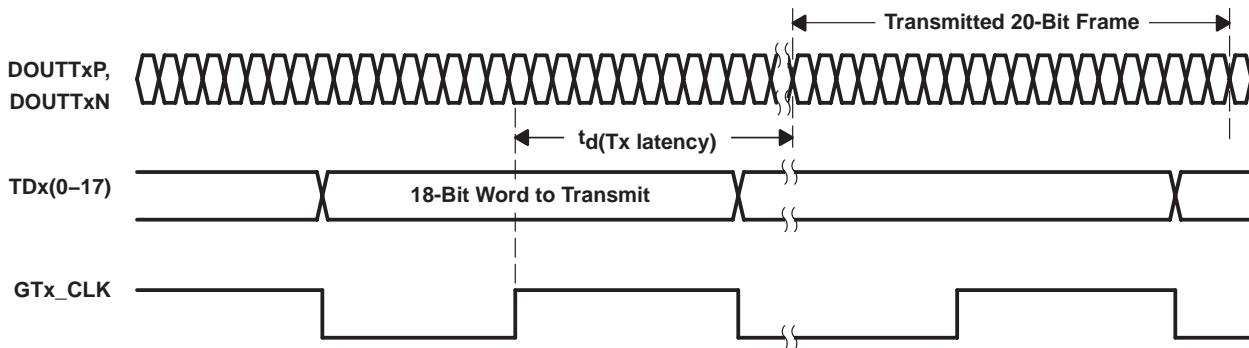


Figure 2. Transmitter Latency

start/stop framing logic

All true serial interfaces require a method of encoding to ensure minimum transition density so that the receiving PLL has a minimal number of transitions in which to stay locked onto the data stream. The signal encoding also provides a mechanism for the receiver to identify the word boundary for correct deserialization. The TLK4120 wraps a start bit (1) and a stop bit (0) around the 18-bit data payload as shown in Figure 3. This is transparent to the user, as the TLK4120 internally adds the framing bits to the data such that the user reads and writes actual 18-bit data.

start/stop framing logic (continued)

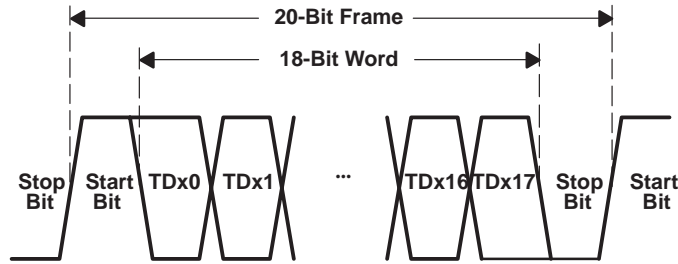


Figure 3. Serial Output Data Stream With Start and Stop Bit

parallel-to-serial

The parallel-to-serial shift register takes in the 20-bit wide frame multiplexed from the framing logic and converts it to a serial stream. The shift register is clocked on both the rising and falling edges of the internally generated bit clock, which is 10 times the GTx_CLK input frequency. The LSB (TDx0) is first out after the start bit as shown in Figure 3.

high-speed data output

The high-speed data output driver consists of a PECL-compatible differential pair that can be optimized for a particular transmission line impedance and length. The line can be directly coupled or ac coupled. See Figure 10 and Figure 11 for termination details. No external pullup or pulldown resistors are required.

The TLK4120 provides a selectable signal preemphasis option for driving lossy media. When signal preemphasis is enabled, the first bit of a run length of same-value bits (e.g., 111...) is driven to a larger output swing, which precompensates for signal inter-symbol interference (ISI) in lossy media, such as copper cables or printed circuit board traces.

receive interface

The receiver portion of the TLK4120 accepts 20-bit framed differential serial data. The interpolator and clock recovery circuit locks to the data stream and extracts the bit rate clock. This recovered clock is used to retime the input data stream. The serial data is then aligned to the 20-bit frame by finding the start and stop bits and the 18-bit data is output on a 18-bit wide parallel bus synchronized to the extracted receive clock (Rx_CLK).

receive data bus

The receive bus interface drives 18-bit wide single-ended TTL parallel data at the RDx[0:17] terminals. Data is valid on the rising edge of Rx_CLK. The Rx_CLK is used as the recovered word clock. The data and clock signals are aligned as shown in Figure 4. Detailed timing information can be found in the TTL output switching characteristics table.

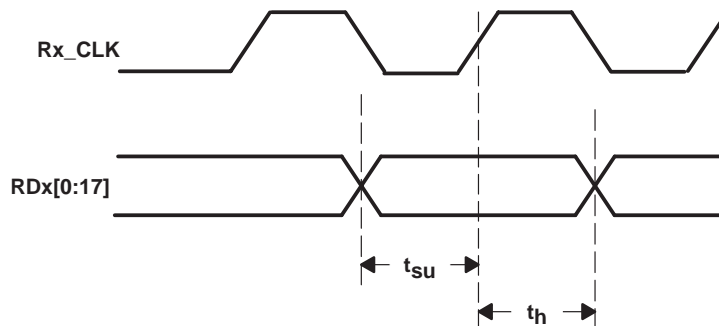


Figure 4. Receive Timing Waveform

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data reception latency

The serial-to-parallel data receive latency is the time from when the start bit arrives at the receiver until the output of the aligned parallel word. The receive latency is fixed once the link is established. However, due to silicon process variations and implementation variables, such as supply voltage and temperature, the exact delay varies slightly. Figure 5 illustrates the timing relationship between the serial receive terminals, the recovered word clock (Rx_CLK), and the receive data bus.

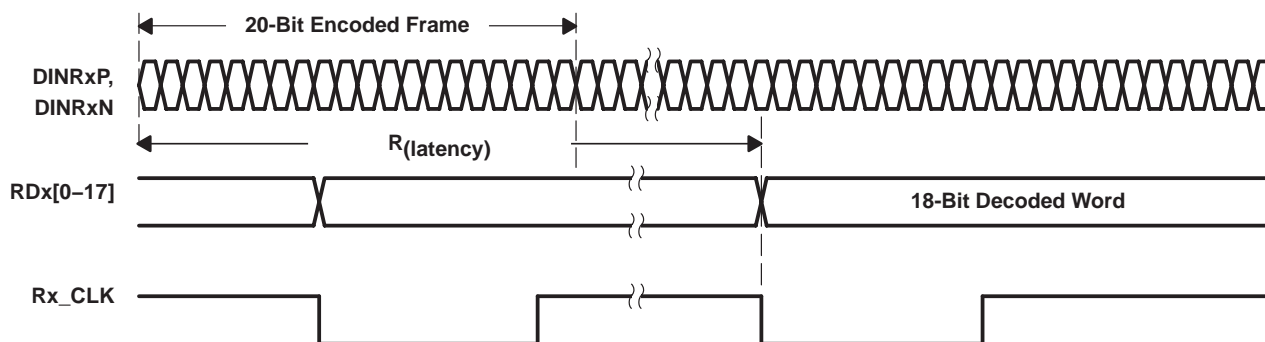


Figure 5. Receiver Latency

serial-to-parallel

Serial data is received on the DINRxP and DINRxN terminals. The interpolator and clock recovery circuit locks to the data stream if the clock to be recovered is within ± 100 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The serial data is then clocked into the serial-to-parallel shift registers.

synchronization mode

The deserializer must synchronize to the serializer in order to receive valid data. Synchronization can be accomplished in one of two ways.

rapid synchronization

The serializer has the capability to send specific SYNC patterns consisting of 9 ones and 9 zeros, switching at the input clock rate. The transmission of SYNC patterns enables the deserializer to lock to the serializer signal within a deterministic time frame. The transmission of SYNC patterns is selected via the SYNC input on the serializer. Upon receiving a valid SYNC pulse (wider than 6 clock cycles), 1026 cycles of SYNC pattern are sent.

When the deserializer detects edge transitions at the serial input, it attempts to lock to the embedded clock information. The deserializer LOCKBx output remains inactive while its clock/data recovery (CDR) locks to the incoming data or SYNC patterns present on the serial input. When the deserializer locks to the serial data, the LOCKBx output goes active. When LOCKBx is active, the deserializer outputs represent incoming serial data. One approach is to tie the deserializer LOCKBx output directly to the SYNCx input of the transmitter. This assures that enough SYNC patterns are sent to achieve deserializer lock.

random lock synchronization

The deserializer can attain lock to a data stream without requiring the serializer to send special SYNC patterns. This allows the TLK4120 to operate in open-loop applications. Equally important is the deserializer's ability to support hot insertion into a running backplane. In the open-loop or hot-insertion case, it is assumed the data stream is essentially random. Therefore, because lock time varies due to data stream characteristics, the exact lock time cannot be predicted. The primary constraint on the random lock time is the initial phase relation between the incoming data and the GTx_CLK when the deserializer powers up.

random lock synchronization (continued)

The data contained in the data stream can also affect lock time. If a specific pattern is repetitive, the deserializer could enter false lock—falsely recognizing the data pattern as the start/stop bits. This is referred to as repetitive multitransition (RMT). This occurs when more than one low-high transition takes place per clock cycle over multiple clock cycles. In the worst case, the deserializer could become locked to the data pattern rather than the clock. Circuitry within the deserializer can detect that the possibility of false lock exists. Upon detection, the circuitry prevents the LOCKBx from becoming active until the potential false-lock pattern changes. Notice that the RMT pattern only affects the deserializer lock time, and once the deserializer is in lock, the RMT pattern does not affect the deserializer state as long as the same data boundary happens each cycle. The deserializer does not go into lock until it finds a unique data boundary that consists of four consecutive cycles of data boundary (start/stop bits) at the same position.

The deserializer stays in lock until it cannot detect the same data boundary (start/stop bits) for four consecutive cycles. Then the deserializer goes out of lock and hunts for the new data boundary (start/stop bits). In the event of loss of synchronization, the LOCKBx terminal output goes inactive and the outputs (including Rx_CLK) enter a high-impedance state. The user's system must monitor the LOCKBx terminal in order to detect a loss of synchronization. Upon detection of loss of lock, sending SYNC patterns for resynchronization is desirable if reestablishing lock within a specific time is critical. However, the deserializer can lock to random data as previously noted. LOCKBx is held inactive for at least nine cycles after loss of lock is detected.

recommended power-up sequence

When powering up the device, it is recommended to first set the ENABLEx terminal low. Set the ENABLEx terminal to high once sufficient time has passed to allow the power supply to stabilize.

power-down mode

When the ENABLEx terminal is deasserted low, the TLK4120 goes into a power-down mode. In the power-down mode, the serial transmit terminals (DOUtxP, DOUtxN) and the receive data bus terminals (RDx[0:17]) go into a high-impedance state.

reference clock input

The reference clock (GTx_CLK) is an external input clock that synchronizes the transmitter interface. The reference clock is then multiplied in frequency 10 times to produce the internal serialization bit clock. The internal serialization bit clock is frequency locked to the reference clock and used to clock out the serial transmit data on both its rising and falling edge clock providing a serial data rate that is 20 times the reference clock.

The receiver tracking logic uses clock phases from the internal PLL as it aligns the recovered clock phase with the incoming serial data stream; therefore, the input reference clock (GTX_CLK) is needed even if the transmit function of the TLK4120 is not being used. The receiver function has the ability to track an incoming serial data stream that is within ± 200 ppm of the data rate that is set by GTX_CLK. This allows the use of clock sources with ± 100 ppm frequency tolerance.

operating frequency range

The TLK4120 may operate at a serial data rate between 0.5 Gbit/s to 1.3 Gbit/s. GTx_CLK must be within ± 100 PPM of the desired parallel data rate clock. Each individual channel may operate at a different rate.

testability

The TLK4120 has a comprehensive suite of built-in self-tests. The loopback function provides for at-speed testing of the transmit/receive portions of the circuitry. The ENABLEx terminal allows for all circuitry to be disabled so that an IDDQ test can be performed.

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loop-back testing

The transceiver can provide a self-test function by enabling (LOOPENx) the internal loop-back path. Enabling this terminal causes serial transmitted data to be routed internally to the receiver. The parallel data output can be compared to the parallel input data for functional verification. (The external differential output is held in a high-impedance state during the loop-back testing.)

power-on reset

Upon application of minimum valid power, the TLK4120 generates a power-on reset. During the power-on reset, the RDx terminals are tri-stated and Rx_CLK is held low. The length of the power-on reset cycle is dependent upon the REFCLK frequency, but is less than 1 ms in duration.

Terminal Functions

| TERMINAL | | TYPE | DESCRIPTION |
|--|------------------------|-----------------------|--|
| NAME | NO. | | |
| DINRAP DINRAN | A6, A7 | Input | Serial receive inputs. DINRxP and DINRxN together are the differential serial input interface from a copper or an optical I/F module. |
| DINRBP DINRBN | F17 G17 | | |
| DINRCP DINRCN | P17 R17 | | |
| DINRDP DINRDN | U4 U3 | | |
| DOUTTAP DOUTTAN | A3 A4 | | |
| DOUTTBP DOUTTBN | C17 D17 | | |
| DOUTTAP DOUTTAN | L17 M17 | | |
| DOUTTDP DOUTTDN | U7 U6 | | |
| ENABLEA ENABLEB ENABLEC ENABLED | H5 E10 M9 J6 | Input (w/pullup) | Device enable. When this terminal is held low, the device is placed in power-down mode. When asserted high while the device is in power-down mode, the transceiver goes into power on reset before beginning normal operation. |
| GTA_CLK GTB_CLK GTC_CLK GTD_CLK | E2 B13 K13 P8 | Input | Reference clock. GTx_CLK is a continuous external input clock that synchronizes the transmitter interface TDx. The frequency range of GTx_CLK is 25 MHz to 65 MHz. The transmitter uses the rising edge of this clock to register the 18-bit input data (TDx) for serialization. |
| SYNCA SYNCB SYNCC SYNCD | F4 D12 N10 K5 | Input (w/pulldown) | Fast synchronization. When asserted high, the transmitter substitutes the 18-bit pattern 111111111000000000 so that when the start/stop bits are framed around the data the receiver can immediately detect the proper deserialization boundary. This is typically used during initialization of the serial link. |
| LOOPENA LOOPENB LOOPENC LOOPEND | H4 D10 P12 M4 | Input (w/pulldown) | Loop enable. When LOOPENx is active high, the internal loop-back path is activated. The transmitted serial data is directly routed internally to the inputs of the receiver. This provides a self-test capability in conjunction with the protocol device. The DOUTTxP and DOUTTxN outputs are held in a high impedance state during the loop-back test. LOOPENx is held low during standard operational state with external serial outputs and inputs active. |

Terminal Functions (Continued)

| TERMINAL | | TYPE | DESCRIPTION |
|-----------|--|---------------------------|---|
| NAME | NO. | | |
| LOCKBA | G5 | Output | Receiver lock. When asserted low indicates that the receiver has acquired bit synchronization on the data stream and has located the start/stop bits so that the deserialized data presented on the parallel receive bus is properly received. |
| LOCKBB | E11 | | |
| LOCKBC | N9 | | |
| LOCKBD | L4 | | |
| PREEMPHA | A5 | Input | Pre-emphasis. When asserted, the serial transmit outputs have extra output swings on the first bit of any run length of save value bits. If the run length of output bits is one, then that bit has larger output swings. |
| PREEMPHB | E17 | | |
| PREEMPHC | N17 | | |
| PREEMPHD | U5 | | |
| RDA(0–17) | A8, B8, C6, C4, D6, D7, D8, D5, E8, E7, E6, F8, F7, E5, F6, G6, F5, E4 | Output (hi-z on power up) | Receive data bus. These outputs carry 18-bit parallel data output from the transceiver to the protocol device, synchronized to Rx_CLK. The data is valid on the rising edge of Rx_CLK as shown in Figure 10. These terminals are high-impedance during power-on reset. |
| RDB(0–17) | H17, H16, F15, D15, F14, G14, H14, E14, H13, G13, F13, H12, G12, E13, F12, F11, E12, D13 | | |
| RDC(0–17) | T17, U17, T16, T15, U16, U15, T14, U14, T13, U12, T12, U11, U10, T11, R10, T9, R9, P10 | | |
| RDD(0–17) | U2, U1, T2, R2, T1, R1, P2, P1, N2, M1, M2, L1, K1, L2, K2, K3, J3, K4 | | |
| RA_CLK | D4 | Output (low on power up) | Recovered clock. Output clock that is synchronized to RDx. Rx_CLK is the recovered serial data rate clock divided by 20. Rx_CLK is held low during power-on reset. |
| RB_CLK | D14 | | |
| RC_CLK | U13 | | |
| RD_CLK | N1 | | |
| TDA(0–17) | A2, A1, B2, C2, B1, C1, D2, D1, E1, F1, F2, G1, H1, G2, J1, H3, J2, J4 | Input | Transmit data bus. These inputs carry the 18-bit parallel data output from a protocol device to the transceiver for encoding, serialization and transmission. This 18-bit parallel data is clocked into the transceiver on the rising edge of GTx_CLK as shown in Figure 9. |
| TDB(0–17) | B17, A17, B16, B15, A16, A15, B14, A14, A13, A12, B12, A11, A10, B11, A9, C10, B9, D9 | | |
| TDC(0–17) | K17, K16, M15, P14, N14, K14, L14, M14, K12, L13, M13, N13, L12, M12, P13, M11, N12, M10 | | |
| TDD(0–17) | U8, T8, R6, P4, P5, R8, P7, P6, M8, N7, N6, N5, M7, M6, N4, L6, M5, K6 | | |
| TESTENA | H6 | Input (w/pulldown) | Test mode enable. This terminal must be left unconnected or tied low. |
| TESTENB | F10 | | |
| TESTENC | P11 | | |
| TESTEND | M3 | | |

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Terminal Functions (Continued)

| TERMINAL | | TYPE | DESCRIPTION |
|---------------|--|--------|---|
| NAME | NO. | | |
| POWER | | | |
| VDD | C8, C12, C14, D3, D11, F3, F9, G4, H15, J12, J13, J16, K15, L5, N3, N8, N11, P15, R4, R13, U9 | Supply | Digital logic power. Provides power for all digital circuitry and digital I/O Buffers. |
| VDDAA | B5, C5 | Supply | Analog power. VDDAx provides a supply reference for the high-speed analog circuits, receiver and transmitter. |
| VDDAB | E15, E16 | | |
| VDDAC | N15, N16 | | |
| VDDAD | R5, T5 | | |
| GROUND | | | |
| GND A | B3, B4, B6, B7, C16, D16, F16, G16, L16, M16, P16, R16, T3, T4, T6, T7 | Ground | Analog ground. GND A provides a ground reference for the high-speed analog circuits RX and TX. |
| GND | B10, C3, C7, C9, C11, C13, C15, E3, E9, G3, G7, G8, G9, G10, G11, G15, H2, H7, H8, H9, H10, H11, J5, J7, J8, J9, J10, J11, J14, J15, J17, K7, K8, K9, K10, K11, L3, L7, L8, L9, L10, L11, L15, P3, P9, R3, R7, R11, R12, R14, R15, T10 | Ground | Digital logic ground. Provides a ground for the logic circuits and digital I/O buffers. |

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

| | |
|--|------------------------------|
| Supply voltage, V_{DD} (see Note 1) | –0.3 V to 3 V |
| Voltage range at TDx, ENABLEx, GTx_CLK, LOOPENx, SYNCx, PREEMPHx | –0.3 V to 4 V |
| Voltage range at any other terminal except above | –0.3 V to $V_{DD} + 0.3$ V |
| Package power dissipation, P_D | See Dissipation Rating Table |
| Storage temperature, T_{stg} | –65°C to 150°C |
| Electrostatic discharge | HBM: 2 kV, CDM: 1.5 kV |
| Characterized free-air operating temperature range | –40°C to 85°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltages, are with respect to network ground.

DISSIPATION RATING TABLE

| Air Flow | 0 m/s | 0.5 m/s | 1 m/s | 2.5 m/s |
|-----------|-------|---------|-------|---------|
| TJA (C/W) | 18.4 | 16.92 | 15.95 | 14.7 |

electrical characteristics over recommended operating conditions

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|-----------|--------------------------------|--|-----|------|-----|------|
| V_{DD} | Supply voltage | | 2.3 | 2.5 | 2.7 | V |
| T_A | Operating free-air temperature | | -40 | | 85 | °C |
| I_{CC} | Supply current | $V_{DD} = 2.5$ V, Rate = 500 Mbps, PRBS pattern | | 180 | | mA |
| | | $V_{DD} = 2.5$ V, Rate = 1.3 Gbps, PRBS pattern | | 460 | | |
| P_D | Power dissipation | $V_{DD} = 2.5$ V, Rate = 500 Mbps, PRBS pattern | | 450 | | mW |
| | | $V_{DD} = 2.5$ V, Rate = 1.3 Gbps, PRBS pattern | | 1150 | | |
| | | $V_{DD} = 2.7$ V, Rate = 1.3 Gbps, worst case pattern | | 1900 | | |
| | Shutdown current | ENABLE = 0, VDDA, V_{DD} terminals, V_{DD} = maximum | | 520 | | μA |
| | PLL start-up lock time | V_{DD} , VDDA = 2.3 V, EN ↑ to PLL acquire | | 0.1 | 0.4 | ms |
| | Data acquisition time | | | 1024 | | bits |

reference clock (GTx_CLK) timing requirements over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|---------------------|-------------------|-----------|-----|-----------|------|
| R_{ω} | Frequency | Minimum data rate | TYP-0.01% | 25 | TYP+0.01% | MHz |
| | | Maximum data rate | TYP-0.01% | 65 | TYP+0.01% | MHz |
| | Frequency tolerance | | -100 | | 100 | ppm |
| | Duty cycle | | 40% | 50% | 60% | |
| | Jitter | Peak-to-peak | | | 40 | ps |

TLK4120

QUAD 0.5 to 1.3 Gbps TRANSCEIVER

SLLS599D – DECEMBER 2003 – REVISED JULY 2007

TTL input electrical characteristics over recommended operating conditions (unless otherwise noted)

TTL Signals: TDx0 ... TDx17, GTx_CLK, LOOPENx, SYNCx, PREEMPHx

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|-------------------------------------|--|-----|-----|------|
| V _{IH} | High-level input voltage | See Figure 6 | | 3.6 | V |
| V _{IL} | Low-level input voltage | See Figure 6 | | 0.8 | V |
| I _{IH} | High-level input current | V _{DD} = Maximum, V _{IN} = 2 V | | 40 | μA |
| I _{IL} | Low-level input current | V _{DD} = Maximum, V _{IN} = 0.4 V | -40 | | μA |
| C _{IN} | Input capacitance | 0.8 V to 2 V | | 4 | pF |
| t _r | GTx_CLK, TDx _n rise time | 0.8 V to 2 V, C = 5 pF, See Figure 6 | 1 | | ns |
| t _f | GTx_CLK, TDx _n fall time | 2 V to 0.8 V, C = 5 pF, See Figure 6 | 1 | | ns |
| t _{su} | TDx _n setup to ↑ GTx_CLK | See Figure 6 | 1.5 | | ns |
| t _h | TDx _n hold to ↑ GTx_CLK | See Figure 6 | 0.4 | | ns |

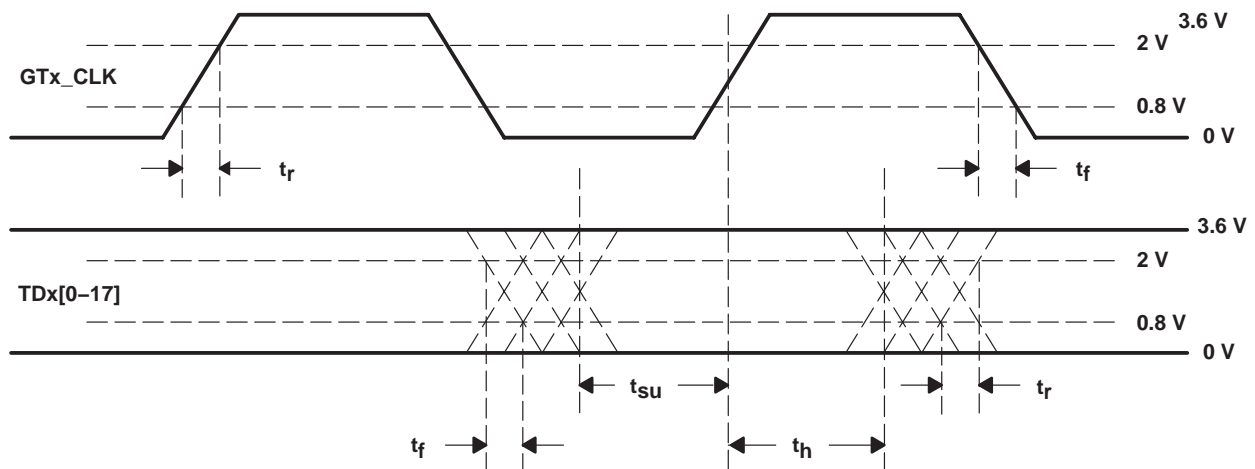


Figure 6. TTL Data Input Valid Levels for AC Measurements

TTL output switching characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|--|--|-----|------|------|
| V _{OH} | High-level output voltage | I _{OH} = -1 mA, V _{DD} = Minimum | 2.1 | 2.3 | V |
| V _{OL} | Low-level output voltage | I _{OL} = 1 mA, V _{DD} = Minimum | GND | 0.25 | 0.5 |
| t _{r(slew)} | Magnitude of Rx_CLK, RDx slew rate (rising) | 0.8 V to 2 V, C = 5 pF, See Figure 7 | 0.5 | | V/ns |
| t _{f(slew)} | Magnitude of Rx_CLK, RDx slew rate (falling) | 0.8 V to 2 V, C = 5 pF, See Figure 7 | 0.5 | | V/ns |
| t _{su} | RDx setup to ↑ Rx_CLK | 50% voltage swing, GTx_CLK = 25 MHz, See Figure 7 | 19 | | ns |
| | | 50% voltage swing, GTx_CLK = 65 MHz, See Figure 7 | 6.7 | | ns |
| t _h | RDx hold to ↑ Rx_CLK | 50% voltage swing, GTx_CLK = 25 MHz, See Figure 7 | 19 | | ns |
| | | 50% voltage swing, GTx_CLK = 65 MHz, See Figure 7 | 6.7 | | ns |

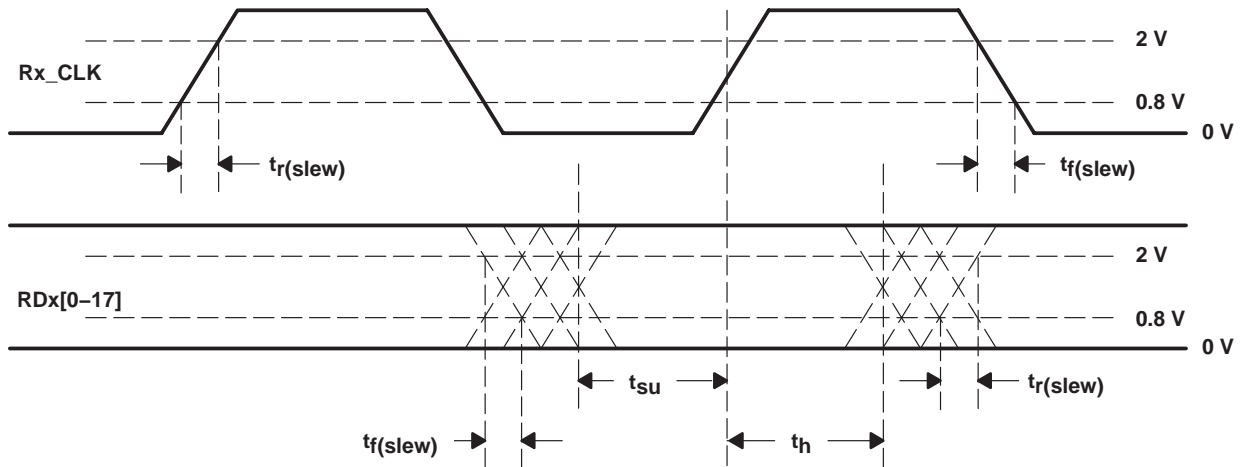


Figure 7. TTL Data Output Valid Levels for AC Measurements

transmitter/receiver characteristics

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---------------------------------|--|---|------|----------------------|------|-----------|
| V _{OD(p)} | V _{OD(p)} = VTXP – VTXN , Preemphasis VOD | DC-coupled. Preemphasis = high, See Figure 8 | 730 | 945 | 1280 | mV |
| V _{OD(pp-p)} | Differential, peak-to-peak output voltage with preemphasis | DC-coupled. Preemphasis = high, See Figure 8 | 1460 | 1890 | 2560 | mV |
| V _{OD(d)} | V _{OD(d)} = VTXP – VTXN , De-emphasis VOD | DC-coupled. Preemphasis = low, See Figure 8 | 560 | 750 | 1100 | mV |
| V _{OD(pp-d)} | Differential, peak-to-peak output voltage with deemphasis | DC-coupled. Preemphasis = low, See Figure 8 | 1120 | 1500 | 2200 | mV |
| V _(cmt) | Transmit termination voltage range, (VTXP + VTXN)/2 | | 1000 | 1250 | 1400 | mV |
| V _{ID} | Receiver input voltage differential VID= RXP – RXN | | 200 | | | mV |
| V _{cmr} | Receiver common-mode voltage range, (VRXP + VRXN)/2 | | 1000 | V _{DD} -350 | | mV |
| I _{in} | Receiver input leakage | | -10 | | 10 | μA |
| C _{in} | Receiver input capacitance | | | | 2 | pF |
| t _r , t _f | Differential output signal rise and fall time (20% to 80%) | R _L = 50 Ω, C _L = 5 pF, See Figure 9 | 100 | 150 | | ps |
| | Serial transmit data total jitter (peak-to-peak) | Differential output jitter, random + deterministic, 2 ²³ -1 PRBS pattern at 1.3 Gbps | | 0.1 | | UI |
| | Receive jitter tolerance | Total input jitter, PRBS pattern, permitted eye closure at zero crossing | | 0.5 | | UI |
| T _{latency} | TX latency | At 500 Mbps | 17 | | 19 | Bit times |
| | | At 1.3 Gbps | 17 | | 20 | |
| R _{latency} | RX latency | At 500 Mbps | 88 | | 92 | Bit times |
| | | At 1.3 Gbps | 90 | | 96 | |

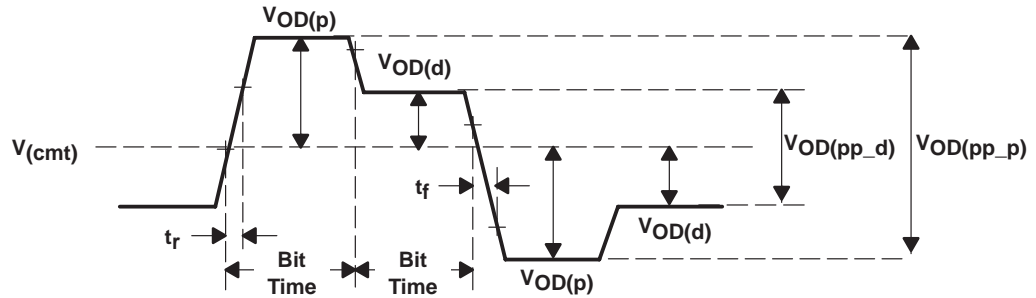


Figure 8. Differential and Common-Mode Output Voltage Definitions

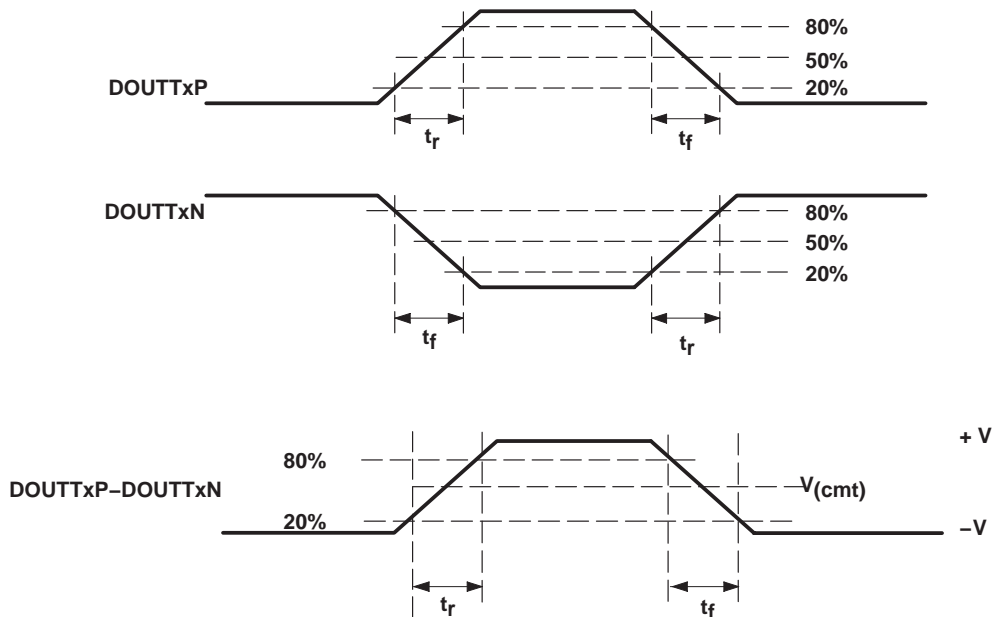


Figure 9. Rise and Fall Time Definitions

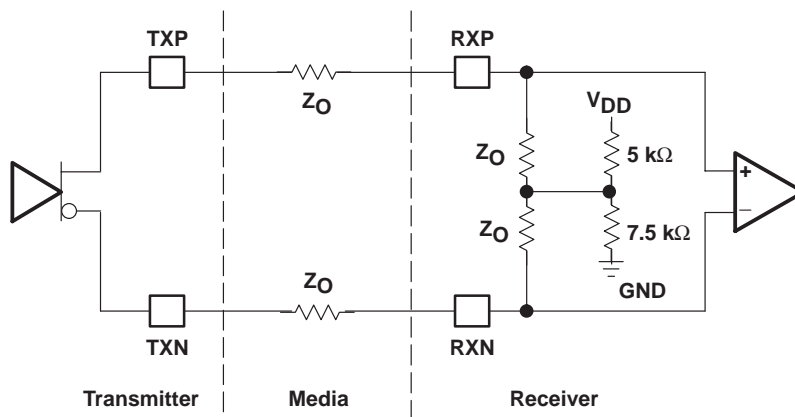


Figure 10. High-Speed I/O Directly Coupled Mode

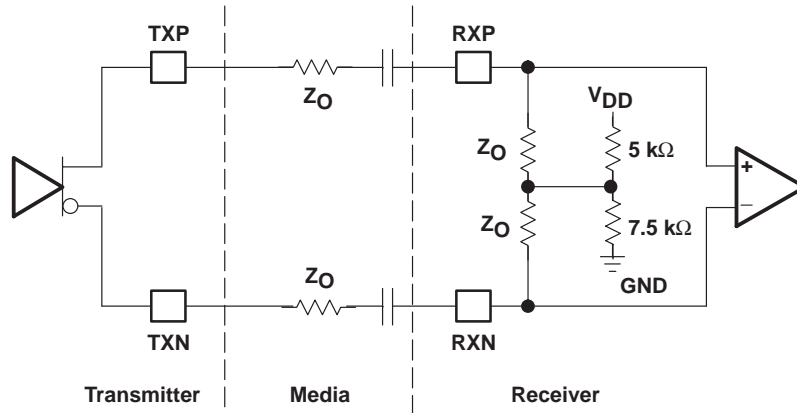


Figure 11. High-Speed I/O AC-Coupled Mode

AC-coupling is only recommended if the parallel TX data stream is encoded to achieve a dc-balanced data stream. Otherwise, the ac capacitors can induce common-mode voltage drift due to the dc-unbalanced data stream.

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TLK4120IGPV | ACTIVE | BGA | GPV | 289 | 84 | TBD | Call TI | Level-3-220C-168 HR |
| TLK4120IZPV | ACTIVE | BGA | ZPV | 289 | 84 | Pb-Free (RoHS) | SNAGCU | Level-3-260C-168 HR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

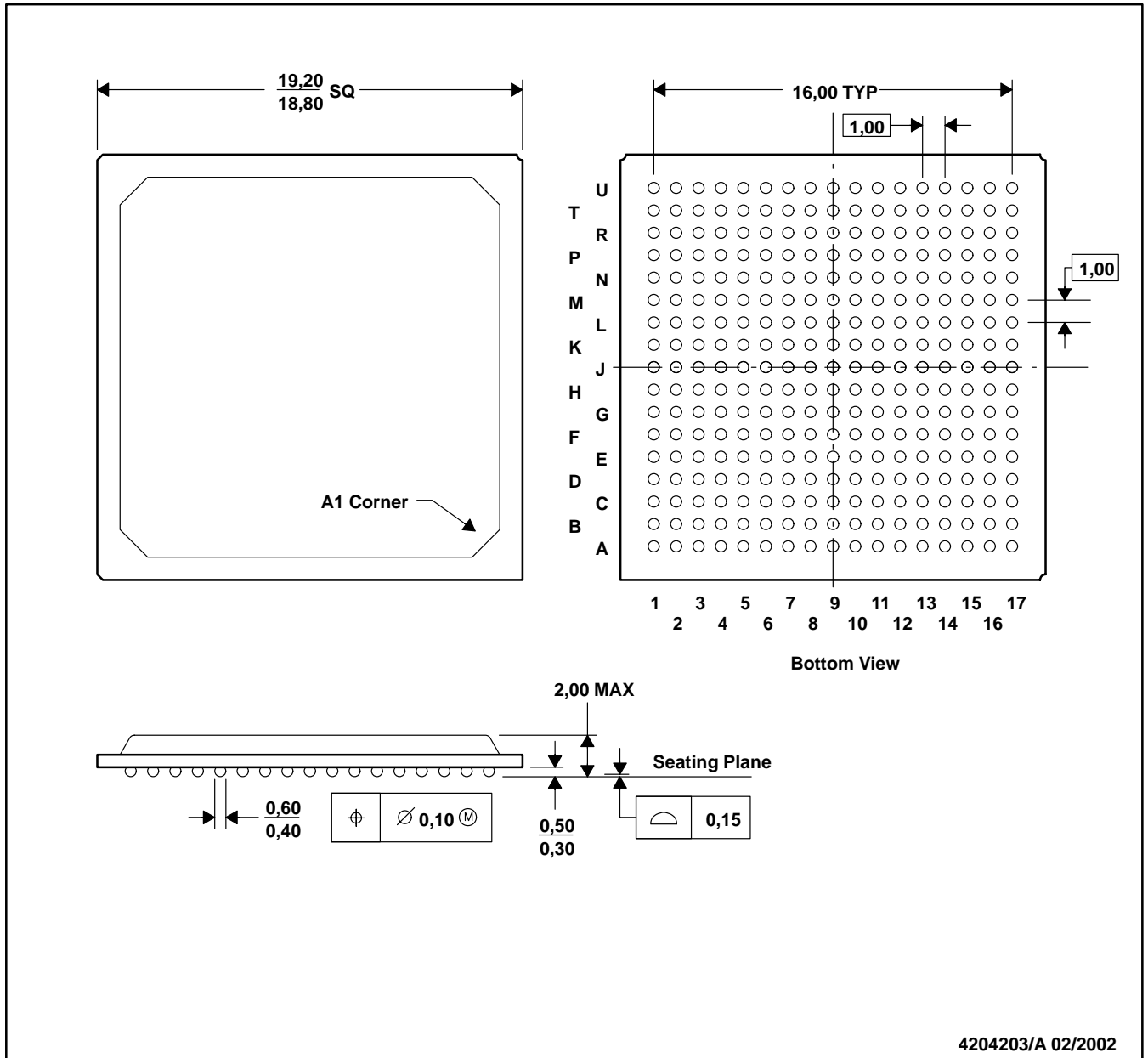
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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GPV (S-PBGA-N289)

PLASTIC BALL GRID ARRAY

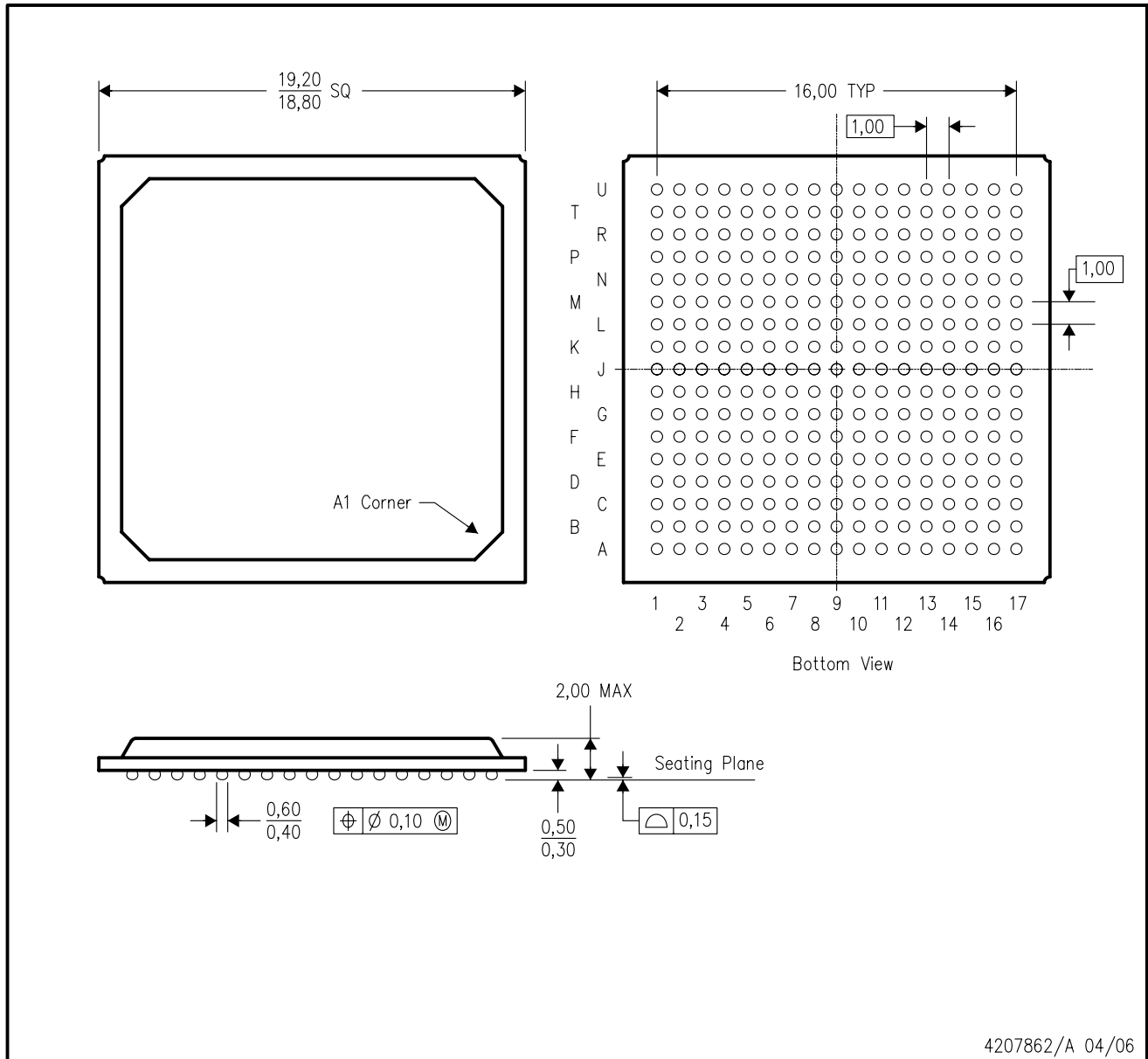


4204203/A 02/2002

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

ZPV (S-PBGA-N289)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. This is a lead-free solder ball design.

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